Abstract – This paper presents a fully integrated, reconfigurable inductance, developed for high-speed power system transient stability emulation. Known active inductance topologies are not suitable for this application for two main reasons. Firstly, most active inductors are used at very high frequencies, due to their RF applications, and secondly, the DC characteristics of active inductors lead to a saturation problem, as a result of offset currents that occur when connecting them in series. Based on a gyrator-C topology, an inductance was realized in a CMOS 0.35\textmu m technology and is detailed in this paper. We were careful to take into account imperfection, calibration, mismatching and process variation. Finally, all requirements were fulfilled to use this inductance in power system AC emulation.

Keywords: analog computation, application specific integrated circuit (ASIC), emulation, microelectronics, power system computation, reconfigurable integrated inductance, transient stability

1 INTRODUCTION

Analog computation for high-speed power system analysis is a continuing field of research [1, 2]. The main advantage of power system emulation over traditional numerical simulators is the faster computation time. Indeed, the computation time is independent of the system size and the model complexity because of intrinsic parallelism. Among others, two different emulation methods, which are both based on the Field Programmable Power Network System (FPPNS) concept [3], are currently under development: the Phasor emulation approach [4] and the AC emulation approach [5, 6]. FPPNS was developed to guarantee high flexibility in emulators. It gains this flexibility by creating an array of atoms, rather than using a fixed power system topology.

Each atom can be programmed to emulate transmission lines, a load and/or a generator, meaning that the same emulator can be used to emulate different topologies. Moreover, not only the atom itself, but also all elements of one atom, are reprogrammable in this method. Fig. 1 illustrates the described concept.

This paper focuses on AC emulation, which was introduced in [5]. AC emulation is based on a one-to-one mapping of components of the real power system (generator, load and transmission line), which is done by emulating their behavior on CMOS active microelectronics. Frequency dependence of the elements is preserved, and the signals propagating on the emulated grid are the shrunk and downscaled current and voltage waves (AC signals) of the real power system. Therefore, this approach is termed AC emulation and can be seen as a downscaling of the real power system on chip. Speed acceleration is obtained by frequency transposition. The emulated power system is working at a much higher frequency (i.e. 500kHz) than the real power system (i.e. 50Hz in Europe), thus ensuring that the emulated phenomena will be much faster (i.e. 10’000 times) than the real ones. The range of phenomena (dynamic or electromagnetic) that can be emulated with an AC emulator depends theoretically only on the chosen generator model. For the first realization, the classical generator model was chosen. Hence the emulator will be limited to the analysis of transient stability. Fig. 2 shows the system level of the first AC atom.

![Figure 1: Field Programmable Power Network System](image1)

![Figure 2: System level of the atom developed for the AC emulation approach (with highlighted inductances)](image2)
The purpose of this work is to develop the reprogrammable, fully integrated inductance, which is used in the AC atom as an internal inductance of the generator model, emulating the transmission line, and as part of the impedance load (cp. Fig. 2).

Currently, inductors are often used in high-speed analog signal processing and data communications. Hence, integrated inductors exist in CMOS fabrication technologies. They can be separated in two groups [7]:

- CMOS spiral inductors (passive)
- CMOS active inductors

Passive inductors are not suitable for our application as they need a prohibitively large silicon area, and have other limitations as a result of their spiral layout. These limitations include a low quality factor and a small and non-tunable inductance. Inductors synthesized using active devices are promising, as they need little area compared to their spiral counterparts. In addition to these, large and reprogrammable inductances with large tuning ranges can be obtained. Nevertheless, the design of any active inductor for power system emulation is not straightforward, as existing topologies are mainly designed for high-frequency applications. A first inductance topology was designed and presented in [5]. In this design, a known topology was adjusted to be suitable for an operation at 500kHz. Only the tuning aspect was considered in the first design. But there is also an offset issue to solve, as well as different imperfections to consider in order to make the use of this inductor possible in power system emulation.

This paper details the inductance topology that has been designed for the application in power system emulation. It starts by explaining the basic concept of the topology. Then, in Section 3, the necessary circuitry for offset limiting is added, and stability and imperfections are discussed. Section 4 is dedicated to tunability and calibration, followed by a presentation of the microelectronic implementation of this inductor. Finally, a transistor-level simulation illustrates the analyzed phenomena and shows the designed inductance working in a two-node power system topology.

2 BASIC CONCEPT

![Figure 3: Floating active inductor (between terminals 1 and 2) based on a gyrator (in black) connected to a capacitor](image)

The developed CMOS inductance is based on a classical gyrator-C topology. One terminal of a gyrator is connected to a capacitor as shown in Fig. 3. A gyrator consists of two back-to-back connected operational transconductance amplifiers (OTAs) and acts as impedance converter.

Therefore, the inductance created with this topology is defined as

\[
L = \frac{2C_m}{G_{m1}G_{m2}},
\]

and can be tuned by changing the capacitor value and/or the transconductance values. The former should be avoided due to the huge silicon area needed to implement a programmable array of capacitances and, in turn, the high ASIC cost. Therefore, the conductances of the OTAs \(G_{m1}\) and \(G_{m2}\) are varied to tune the inductance.

Due to the nature of synthesized devices, the frequency range of active inductors is limited. In order to analyze the frequency range of the inductor depicted in Fig. 3, the behavior of the OTA has to be fully understood.

Basically, an OTA converts the voltage difference at its input in a current through its transconductance. Fig. 4a shows an equivalent OTA model where only the dominant pole is taken into account. The following equations for the output current \(i_{out}\), the voltage gain \(A_i\) and the dominant pole \(f_{dp}\) apply:

\[
\begin{align*}
\text{(2)} & \quad i_{out} = -G_m \cdot V_{in}, \\
\text{(3)} & \quad \frac{V_{out}}{V_{in}} = A_i = \frac{G_m R_{out}}{1 + j \omega C_{out} R_{out}}, \\
\text{(4)} & \quad f_{dp} = \frac{1}{2\pi C_{out} R_{out}}.
\end{align*}
\]

All parameters are illustrated in Fig. 4a.

![Figure 4: (a) one-pole equivalent model (b) two-pole equivalent model of an OTA](image)

Whenever the non-dominant pole needs to be considered, an extended equivalent model is used. It is depicted in Fig. 4b. The operation of an OTA is then characterized by the following equations:

\[
\begin{align*}
\text{(5)} & \quad i_1 = -G_m \cdot V_{in}, \\
\text{(6)} & \quad i_{out} = -\frac{1}{R_p} \cdot V_i, \\
\text{(7)} & \quad \frac{V_{out}}{V_{in}} = A_i = \frac{G_m \cdot R_{out}}{(1 + j \omega C_{out} R_{out})(1 + j \omega C_p R_p)}, \\
\text{(8)} & \quad f_{dp} = \frac{1}{2\pi C_{out} R_{out}}.
\end{align*}
\]
Using this background, the equivalent impedance of the gyrator-C topology can be determined. Fig. 5 depicts the bode plot of the asymptotes of its equivalent impedance using the one-pole model for the two OTAs of the gyrator. The two OTAs are labeled with suffix 1 and 2, respectively. The frequency range limitation is clearly visible. The inductance operating range is limited between the zero frequency \( \omega_z \) and the resonance frequency \( \omega_n \).

\[
\omega_z = \frac{1}{(C_1 + C_{out})R_{out}}
\]

Figure 5: Bode plot (asymptotes) of the active inductor’s impedance and of the corresponding \( RL \)-transmission line

\( C_{out,1,2} \) and \( R_{out,1,2} \) are the output resistance and capacitance of OTA1 and OTA2, respectively. All other variables are defined in Fig. 3. The more ideal the OTAs are, the larger the frequency range of the inductance is. Therefore, the OTAs should be designed to have a large \( R_{out} \) and a small \( C_{out} \).

Outside of this range, other elements become dominant. Indeed, the equivalent impedance of the active inductance consists of several additional parasitic elements, under which is a small resistance in series with the inductance. The whole equivalent impedance is illustrated in Fig. 6.

Figure 6: Complete equivalent active inductance model

### 3 ADDITIONAL ASPECTS

#### 3.1 Offset

Additional circuitry is needed in order to control the operating point (OP) of the active inductor. Indeed, as is highlighted in Fig. 5, the active inductor behaves like a resistor at the DC operating point; this means that an offset voltage induces an offset current that is able to saturate the inductance. The voltage source, in series with the equivalent impedance, models this phenomenon (see Fig. 6). Ideally, the offset voltage is equal to zero, but in reality there is statistically always a non-zero offset due to mismatch. Therefore, there will be a voltage drop \( \Delta V_{OP} \) between the terminals of the inductor.

\[
V_m = G_{out} R_{out} \Delta V_{OP} = A_{11} \Delta V_{OP},
\]

This voltage drop leads to a voltage \( V_m \) at the output of the gyrator that equals

\[
V_m = G_{out} R_{out} \Delta V_{OP} = A_{11} \Delta V_{OP},
\]

a value that saturates very quickly. Hence it is of utmost importance to control the OP of \( V_m \). This is done by adding an additional block to the inductor topology (cp. Fig. 7).

Figure 7: Active inductor with control block and its equivalent impedance model

This block senses the DC voltage component of \( V_m \) and compares it to the ideal value and then calibrates the current output of OTA1. The equivalent model of the block is depicted in grey in Fig. 9.

The equivalent impedance of the active inductor changes as a supplementary pole, and zero is added by the compensation block (cp. Fig. 8). A complex conjugate zero, a complex conjugate pole and a simple pole characterize the impedance of the modified version of the active inductor. The operating frequency of the inductor is now delimited by the dip frequency of the complex conjugate zero \( \omega_{z,1} \) and the peak frequency of the complex conjugate pole \( \omega_{z,2} \).

\[
\omega_{z,1} = \frac{G_{m} G_{c} + \frac{1}{R C_{out}}}{R C_{out}}
\]

\[
\omega_{z,2} = \frac{G_{m} G_{c} + \frac{1}{R C_{out}}}{R C_{out}}
\]

Figure 8: Bode plot (asymptotes) of the modified inductor’s impedance (refer to Fig. 9 for the variable definitions) and of the corresponding \( RL \)-transmission line

This is portrayed in Fig. 7 by adding an \( RC \)-impedance in series to the original impedance model. This \( RC \)-impedance has two main functions. First, it increases the resistance at the DC operating point, thereby limiting the offset current and hence limiting the offset voltage. The voltage source in the model becomes a controlled voltage source. Second, it short-circuits the added resistance for higher frequency, thus guaranteeing that the operating range of the inductance remains the same.

#### 3.2 Stability

An open-loop analysis is necessary to examine the stability of the inductance. The equivalent open-loop
model of the modified inductance is illustrated in Fig. 9. Fig. 10 pictures the Bode plot (phase and module asymptotes) of the open-loop voltage transfer function

\[ H(j\omega) = \frac{V_{\text{out}}}{V_{\text{in}}} \tag{11} \]

The zero \( \omega_2 \) is due to the control block and is defined as

\[ \omega_2 = \frac{1}{RC} \tag{12} \]

And the resonance frequency and the poles are

\[ \omega_n = \sqrt{\frac{1 + G_{m1}R_{\text{ort1}}}{RC(C_L + C_{\text{ort1}})R_{\text{ort1}}}}, \tag{13} \]

\[ \omega_p1 = \frac{1}{R_{\text{ort2}}C_{\text{ort2}}} \tag{14} \]

and

\[ \omega_p2 = \frac{1}{R_pC_p}. \tag{15} \]

All variables used in (11-15) are defined in Fig. 9.

![Figure 9: Equivalent open-loop model of the inductance with control block (in grey)](image)

![Figure 10: Bode plot of the equivalent open-loop model simulated with Spectre (Cadence)](image)

An analysis of these equations permits the following conclusions:

- The resonance frequency \( \omega_n \) is not influenced by the parasitic pole and the output pole.
- The stability depends on the dominant pole frequency of OTA\(_2\) and the non-dominant pole frequency of OTA\(_1\).
- The peak frequency of the complex conjugate pole \( \omega_2 \) is equal to the dip frequency of the complex conjugate zero \( \omega_k \) in Fig. 8, i.e. the lower limit of the operating frequency range of the inductance.
- Closing the feedback loop creates the complex conjugate pole \( \omega_{k2} \) seen in Fig. 8.

### 3.3 Large common mode variation

Another undesirable effect is a parasitic sinusoidal current. This current appears because of the big common mode voltage variation on each terminal of the inductance, and the small voltage difference between the terminals (typical behavior of a transmission line). Such behavior at the input of an OTA generates a varying voltage at a current mirror output. This leads to the described parasitic current. To be sure that this current is negligible, the emulated per-unit (p.u.) current that is chosen should be high, and the current mirror has to be designed to minimize this error.

### 4 RANGES AND CALIBRATION

The above analysis and a few other aspects allow the choosing of shrink and downscaling factors from the real power system components on the emulated power system components (see Table 1). Out of these results the tuning range needed for the inductance is extracted.

<table>
<thead>
<tr>
<th>[p.u.]</th>
<th>real world</th>
<th>emulated world</th>
</tr>
</thead>
<tbody>
<tr>
<td>( U )</td>
<td>1</td>
<td>800kV</td>
</tr>
<tr>
<td>( I )</td>
<td>1</td>
<td>400mA</td>
</tr>
<tr>
<td>( S )</td>
<td>1</td>
<td>3200VA</td>
</tr>
<tr>
<td>( Z )</td>
<td>1</td>
<td>20kΩ</td>
</tr>
<tr>
<td>( f )</td>
<td>---</td>
<td>500kHz</td>
</tr>
</tbody>
</table>

**Table 1:** Real vs emulated world

In our case, the transposed frequency was set to 500kHz, meaning that the emulated phenomena would be 10’000 times faster than the real-world phenomena. Choosing 500kHz ensured that no RF design challenges were added, and that enough gain bandwidth could be obtained with commonly used amplifier topologies keeping a maximal speed enhancement. The voltage and current downscaling factors were chosen with care, in order to minimize the influence of the imperfections mentioned in Subsection 3.3. The per-unit voltage was kept as small as possible in order to minimize the parasitic current. At the same time, the per-unit current was maximized keeping reasonably high per-unit impedance: The higher the impedance, the better the stability of the inductance (cp. analytical analysis of the inductance).

<table>
<thead>
<tr>
<th>( \frac{L}{ \text{Transmission line, } L} )</th>
<th>range</th>
<th>( L_{\text{min}} [\text{mH}] )</th>
<th>( L_{\text{max}} [\text{mH}] )</th>
</tr>
</thead>
<tbody>
<tr>
<td>50-450km</td>
<td>0.15</td>
<td>1.4</td>
<td></td>
</tr>
<tr>
<td>( \text{Internal inductor, } X'd )</td>
<td>0.2-0.4p.u.</td>
<td>1.27</td>
<td>2.55</td>
</tr>
<tr>
<td>( \text{Reactive load, } L_t )</td>
<td>0.02-0.4p.u.</td>
<td>0.158</td>
<td>2.55</td>
</tr>
</tbody>
</table>

**Table 2:** Inductance ranges

Table 2 specifies the emulated inductance ranges of the different power system components. Thus, the tuning range of the inductance should be from 0.15 to 2.55mH and hence the transconductance \( G_{m1} \) and \( G_{m2} \) ranges are determined using (1).
In this scope, $C_L$ was fixed at 15pF, a reasonable value in terms of area ($32'500\mu m^2$, 30% of the total inductor area). The related transconductance values were also considered before deciding upon the capacitor value. The transconductance of an OTA depends on the current flowing through its input transistors and the ratio width over length (W/L) of these transistors. After the integration, only the current can be varied: the dimensions are fixed. Fig. 11 illustrates these relations. Finally, it was decided to vary only $G_{m1}$ and to fix $G_{m2}$ at a constant value. Two main reasons led to this decision:

1. Varying the current in the OTA also affects its poles. Therefore, as illustrated in Fig. 10, in order to guarantee stability, the dominant pole of the second OTA has to be at the highest possible frequency.

2. As we want to emulate short circuits on transmission lines, the second OTA has to be able to sink/source a lot of current. Therefore, it is best to keep this current constant at 7.5p.u. for every inductance.

![Figure 11: Relation between transconductance, current and width over length ratio (W/L) of a PMOS transistor](image)

The transconductance of OTA$_1$ $G_{m1}$ is therefore the only parameter to be varied and - keeping $C_L$ and $G_{m2}$ constant - $G_{m1}$ has to be tunable by a factor of 17. This variation is purely theoretical as process, and mismatch variations were ignored. Indeed, a passive integrated poly capacitor can vary up to ±30%, while the transconductance differs up to ±20%. These variation ranges have to be compensated using a larger $G_{m1}$ tuning range, i.e. a larger current variation range. This means that the inductance values have to be calibrated on chip. In this scope, at least the precise capacitor value of $C_L$ has to be known and the current and voltage sine waves passing through one reference inductor on the chip have to be measured. Another possibility for calibration is to measure each inductance separately $G_{m1}$, $G_{m2}$ and $C_L$. So as not to further boost the inductance topology, the former solution was chosen for the first ASIC realization.

**5 REALIZATION**

Table 3 summarizes the most important facts about the transistor-level realization of the inductance. All values are given without considering the current biasing structure, and only typical values are listed. In fact, the current in OTA$_1$ can vary between 0.5μA and 50μA. This is necessary to maintain the inductance range in the case of extreme process variations, as it was described in the previous section.

The realized inductance can finally be varied between 600μH and 5mH. A second version of the inductance has to be created to cover the lower inductance values. In doing this, special attention must be paid to stability. Indeed, for the current inductor, stability cannot be guaranteed at high currents (= high $G_{m1} =$ low inductance).

<table>
<thead>
<tr>
<th>Technology</th>
<th>CMOS AMS 0.35μm, Supply voltages 3.3V and 0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topology</td>
<td>Current</td>
</tr>
<tr>
<td>OTA$_1$</td>
<td>Folded cascode with linearized differential pair [8]</td>
</tr>
<tr>
<td>OTA$_2$</td>
<td>Simple OTA [8]</td>
</tr>
<tr>
<td>R</td>
<td>Simple OTA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Inductance</th>
<th>Area</th>
<th>Power consumption</th>
<th># transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>105'400μm$^2$</td>
<td>2mW @ $I_{\text{max}}$</td>
<td>61</td>
<td></td>
</tr>
<tr>
<td>$C_L$</td>
<td>$32'500μm^2$</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>$C$</td>
<td>$32'500μm^2$</td>
<td>---</td>
<td>---</td>
</tr>
</tbody>
</table>

Table 3: Summary of the realized CMOS active inductor

Commonly used OTA topologies were chosen. Even the resistance $R$ of the compensation block was implemented with a simple OTA in order to save area. Indeed, an active 15MΩ resistance occupies only about 1% of the area of an equal-value, passive, high-resistivity poly resistance.

As the current in OTA$_1$ has to vary by a factor of 100, the differential pair had to be linearized to optimize its linearity.

![Figure 12: Micrograph of the realized ASIC](image)

A micrograph of the realized ASIC is shown in Fig. 12. The ASIC is under test. The complete chip area is 12.43mm$^2$ and the following blocks were implemented on it:

1. A fixed power system topology with 2 generators and 2 transmission lines.
2. A current biasing block, which locally creates all constant currents needed to bias the inductors.
3. An array of eight matched 15pF capacitors needed as conversion capacitors \( C_L \) of the inductors.
4. A capacitor measurement block in order to determine the precise value of the \( C_L \) capacitors.
5. A current copy amplifier to be tested separately.
6. 2 inductors connected in series in order to test the offset limiting issue.
7. 1 inductor to be tested and characterized separately, including the necessary buffers to connect external voltage sources and measure the current at the terminals of the inductor.

6 SIMULATIONS

6.1 Description of the simulation method

The simulation method used here consists of the use of the Spectre simulator of Cadence [9]. This allows the simulation of the transistor level of the designed inductance, as well as the analysis of the influence of process variations and mismatch; this latter is done either by doing corner analysis (worst-case approach) or by Monte Carlo simulations (statistical variations of the device parameters). Behavioral simulations are also possible, using a functional library containing ideal elements.

6.2 AC analysis

First a single inductor is analyzed. Fig. 13 shows the Bode plot of the equivalent impedance for a 1.5mH inductance for different corner simulations (typical case \( tm \), worst speed case \( ws \) and worst power case \( wp \)). The operating range of the emulator is highlighted.

![Figure 13: Equivalent impedance (module and phase) for an inductance \( tm/ws/wp \) of 1.5mH with highlighted operating range](image)

The current is calibrated in order to obtain in each simulation case an inductance of 1.5mH. Note the big difference between the two extreme cases \( wp \) and \( ws \).

Doing the same simulation for the smallest and biggest inductance values \( L_{\text{min}} \) and \( L_{\text{max}} \) shows that in the most extreme situation the phase error can reach 5 degrees at 500kHz compared to an ideal inductance.

6.3 OP analysis

The purpose of second simulation is to check that the designed inductance is able to find appropriate operating points in each possible case. To this end, two inductances were connected together and the voltage at their connection point \( V_{\text{middle}} \) was observed. Fig. 14 depicts the test configuration. A Monte Carlo analysis shows that the compensation block fixes a good operating point for each possible offset (cp. Fig. 15).

![Figure 14: Test configuration for operating point verification](image)

At the same time we also observed the offset current produced by the compensation block \( (I_1, I_2, I_3) \). It is never higher than 4.5μA. This value is small enough compared to the max sink/source current of the inductance.

6.4 Simple power system topology

In this simulation the inductance is tested in its final context. A simple topology consisting of two generators \( G_1 \) and \( G_0 \) connected together through a transmission line was chosen. This is the topology implemented on the first realization. In order to validate the developed models, simulations with more nodes have been performed and are presented in [6].

\( G_1 \) is based on the classical generator model and \( G_0 \) is a slack generator. The topology and the component’s characteristics are shown in Fig. 16.

![Figure 16: Emulated power system topology with its characteristics in p.u.](image)

As a reference scenario, a short circuit of 7μs (corresponds to 70ms in the real world) at the beginning of the transmission line is emulated. Fig. 17 compares the results of a purely behavioral emulation to partial transistor-level emulation. In the latter only the inductances were replaced by their transistor level; the generators remain behavioral. This comparison validates the designed inductance. Only a small difference is visible.
This difference can be expected due to the error on the phase (≠ 90 degrees on the whole range) and the presence of parasitic capacitances.

Indeed, the three main power system component models contain inductors (transmission line, generator and load model). A commonly used active inductance topology was not suited for power system emulation, as the specifications needed do not match: the voltage is not fixed at its terminals and there is a large common mode variation. These environmental constraints introduce design constraints. The former requires the addition of another block and the latter delimitates the downscaling factors. In addition to these limitations, the inductor was designed taking into account possible technology variations. This is important because integrated passive elements can vary up to 30%. These possible variations have to be absorbed by calibration.

The designed inductance was realized. The area of one inductance is 0.1mm² and the power consumption at maximal current is 2mW. Currently, the integrated inductance is under test. But transistor-level simulations presented in this paper confirmed its functionality and highlighted different design aspects.

REFERENCES