

# MIXED-SIGNAL COMPUTATION HARDWARES DEDICATED TO HIGH-SPEED DYNAMIC POWER SYSTEM EMULATION

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**Abstract**—This paper examines two mixed-signal hardware circuits dedicated to transient power system emulation. They both use a flexible, modular and very high-speed emulation approach based on a field programmable power network system (FPPNS). This promising approach is dedicated to emulate multiple nodes power system dynamics. The speed limit of such approach overcomes the numerical simulators because of the system intrinsic parallelism. Both circuits can be plugged into the same hardware platform and the accuracy of the results are compared with a reference power system simulator. Details on the designed hardware are given in this paper. The promising results of both circuits show that the design of a fully integrated solution containing an array of 100 power system nodes can be achieved.

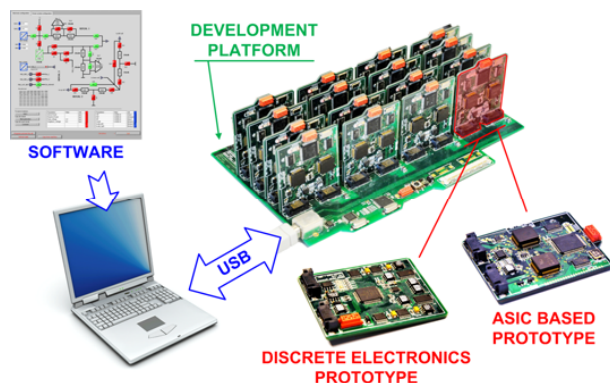
**Keywords:** *high-speed computation, security assessment, mixed-signal circuit, emulation, ASIC.*

## 1 INTRODUCTION

New requirements for power grids are needed and power grid towards a smart grid is in progress. Indeed, power consumption has been steadily increasing and is still increasing. Therefore the power grid operates nearer and nearer its operating limits. Focus is put on renewable energy leading to a much more complex and less predictable power grid.

It is fundamental to establish a very high-speed power system simulator which enables online security assessment [5]. Such simulator could be combined with economic and ecologic aspects to guarantee ideal and instantaneous decision making. Existing digital simulators, which are nowadays used by power system operators, are too slow for faster-than-real-time simulation. Speed can be enhanced by means of dedicated hardware architectures. A promising architecture based on analog computation has been proposed in the past [1], which aims for a dedicated analog computer realized as very large system integrated (VLSI) circuit. This approach was however very limited in terms of flexibility and models. In [2] an emulation approach, called Phasor Emulation (PE), was introduced that aims to overcome these limitations by means of massive parallel architectures implemented using mixed-signal computation. A first prototype confirmed the feasibility of emulation as well as its high computation speed capabilities. Indeed the presented emulator was 100 times faster than real time (emulated behavior speed is 100 times faster than real behavior speed). Furthermore, loss of precision compared to purely numerical simulators can be strongly reduced using advanced circuit techniques allowing automatic calibration.

This paper presents two novel printed circuit board (PCB) prototypes of the mentioned PE approach. Both aim to confirm the feasibility of a mixed-signal emulation based on the PE approach. Moreover both prototypes can be plugged onto the same development platform (Fig. 1). Comparison of results is therefore easy and can be done by same software. PCB prototypes nonetheless differ in their electronic components. Indeed, the first prototype has been designed with discrete electronic components. The second prototype is based on a new application specific integrated circuit (ASIC) dedicated to PE approach. It improves the discrete electronics limitation in terms of area and signal-to-noise ratio. This second prototype anticipates the realization of a multi-node power system on chip (SoC).



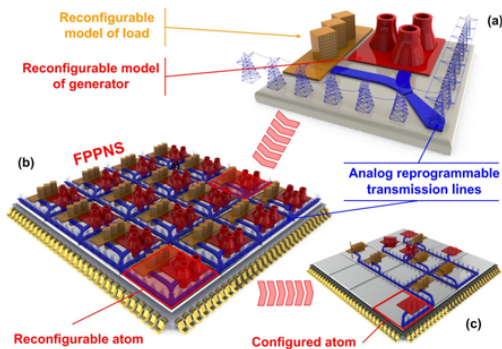
**Figure 1:** Overview of the system containing the development platform and both novel pluggable hardware prototypes.

This paper is organized as follows. We start by describing the system architecture we developed to guarantee the high flexibility of our analog power system emulator. Then, we present the architecture of the PE approach and go into the theoretical principles. Afterwards, a first set of generator and load models that can be implemented on our hardware is presented and validated by comparing results with EUROSTAG. Then, both PCBs are presented as well as our new ASIC. Finally, emulation results of this hardware are provided and validated by comparing with digital reference simulations and the results are discussed.

## 2 AN ARRAY OF RECONFIGURABLE POWER SYSTEM NODES

A new design concept dedicated to power system emulation has been developed in order to make our dedicated analog computer as flexible as possible in terms of topology. This concept is based on a modular array of power

system nodes (atoms) that can be programmed to any power system topology. It is called field programmable power network system (FPPNS). Each atom can be configured either as a generator, as a load or both. Moreover, such an atom also contains analog reprogrammable components emulating the transmission lines of the power grid. Fig. 2 shows a single atom (a) and an array of atoms (b) (c) to illustrate the described concept.



**Figure 2:** (a) A conceptual view of one reconfigurable power system node (atom) (b) Array of 16 atoms. (c) Programmed array of atoms.

### 3 ANALOG EMULATION PRINCIPLE

Digital computation dedicated to time domain transient stability simulation uses the inverse admittance matrix of the grid in order to link node voltages to currents that flow in the grid. Matrix equations linking current and voltage need to be computed at each time step when solving dynamics problem. Therefore, computation time is a square function of the simulated matrix size. Moreover differential algebraic equations (DAE) are computed in the same time and for each node in order to simulate the behavior of the generators and the loads, decreasing at the same time the computation speed.

The analog computation approach of the grid is a mapping between the real grid and the analog emulated grid. Hence the heavy matrix calculation is replaced by an instantaneous analog computation of the grid. Grid emulation can therefore be described as an intrinsic and massive parallel method to compute the grid equations.

#### 3.1 Emulation approaches

Two different emulation approaches can be identified. The first one is the so called PE approach. It allows the analog computation of both complex currents and complex voltages in the grid by means of analog computation. The complex nature of the grid components is mathematically replaced by separated equivalent resistive network. The second one is called the AC emulation approach [3]. It is a downscaled model of the real power system where the nature of each grid component is preserved and the frequency is greatly increased.

#### 3.2 Architecture candidates

The architecture of analog emulators can be realized in two ways: using mixed-signal architecture or full analog architecture. Mixed-signal architecture (analog and digital

computation) means that the grid equations are computed by means of high bandwidth programmable analog components and the generator and load equations are computed using digital processors. A high-speed digital-to-analog converter (DAC) as well as analog-to-digital converter (ADC) allows the linking analog and digital domains.

Such emulation keeps the advantage of pure analog computation where computation time is not dependent of the number of nodes [6]. In addition, the complexity and flexibility of the models can be greatly increased with the use of digital processors for the load and generator models. Moreover, the digital processing dedicated to solve load and generator model can be easily parallelized on low-cost processors connected to load or generator using the dedicated interface. Therefore each atom contains the necessary interface to connect the digital processors. It also contains the programmable blocks which connect each atom together for computing the grid equations analogically. Nevertheless, the speed of a mixed-signal architecture mainly depends on the DAC and ADC conversion speed [2].

A full analog architecture means that the overall computation blocks are realized with analog electronic blocks. In a purely analog emulator the computation speed depends on the bandwidth of the analog components that emulate the grid, the generator and the load models [3]. This speed and accuracy limitation is mainly due to the capacitive parasitic effects of the used technology. Therefore, an FPPNS realized with a full analog architecture is probably faster than a mixed-signal architecture. Nevertheless, a full analog architecture is much more limited in terms of flexibility and suffers from a much more intensive calibration process before starting a set of emulations. Finally, the design process of a fully integrated analog emulator is much longer for the same process than for a mixed-signal architecture.

For those reasons the authors have chosen the mixed signal architecture in order to validate the FPPNS concept. They also choose the phasor emulation approach in order to compute the grid equation analogically. The next chapter is therefore related to the grid model.

## 4 THE PHASOR EMULATION (PE) APPROACH

### 4.1 Grid model

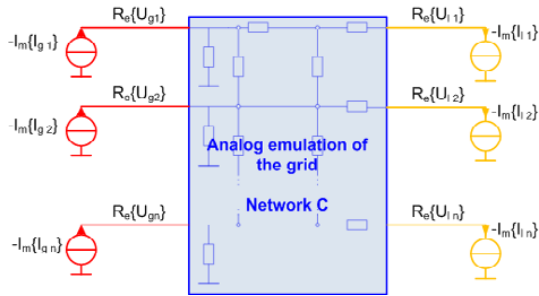
Both PCB implementations are based on the PE approach. As described above it uses a complex representation of voltages and currents magnitudes. The relation that links voltages to currents is given by the admittance of the grid. Multiple and isolated networks (A, B, C and D) are realized in order to emulate this complex representation and this are mathematically illustrated in (1). Those networks allow separate emulation of the real and imaginary part of the current flowing in the grid. Consequently the use of purely resistive components becomes possible for emulating the RLC  $\pi$ -lines building the grid. Hence this mathematical model is easily implemented using a high resistivity layer of major CMOS submicron processes.

When modeling high-voltage transmission lines the serial resistive part  $R_{ij}$  of the  $\pi$ -line can be neglected in comparison to the inductive part. Hence, only inductive

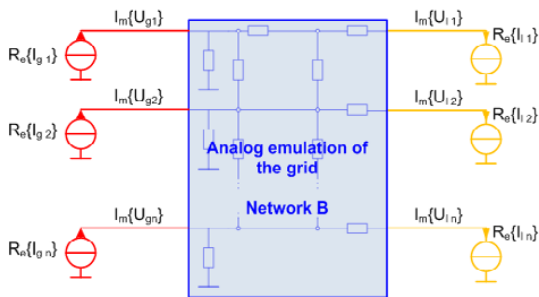
part  $X_{ij}$  is taken in consideration. Therefore the complex current that flows through transmission lines is directly linked to the complex voltage magnitude and the inductive part of the line; Network A and Network D shown in (1) can be neglected thanks to the superposition of the current. Only complex currents related to  $X_{ij}$  in Network B and Network C are considered.

$$\begin{aligned} \underline{I} &= \Re\{ \underline{I} \} + j \cdot \Im\{ \underline{I} \} \\ &= \underbrace{\sum_{j=1}^n \left( \frac{R_{ij}}{R_j^2 - X_j^2} \cdot \Re\{ \underline{U}_j \} \right)}_{\text{Network A}} + \underbrace{\sum_{j=1}^n \left( \frac{X_{ij}}{R_j^2 - X_j^2} \cdot \Im\{ \underline{U}_j \} \right)}_{\text{Network B}} \\ &\quad - \underbrace{j \cdot \sum_{j=1}^n \left( \frac{X_{ij}}{R_j^2 - X_j^2} \cdot \Re\{ \underline{U}_j \} \right)}_{\text{Network C}} + \underbrace{j \cdot \sum_{j=1}^n \left( \frac{R_{ij}}{R_j^2 - X_j^2} \cdot \Im\{ \underline{U}_j \} \right)}_{\text{Network D}} \end{aligned} \quad (1)$$

The real part of the voltage is linked to the imaginary part of the current in the network C. Conversely, the imaginary part of the voltage is linked to the real part of the current in the Network B. Therefore, one ends up with two entirely separated but topologically equivalent networks where the networks are linked together only through the loads and generators nodes. Both relations are schematically shown in Fig. 3 and Fig. 4 where networks B and C represent two topologically equivalent matrices of resistances. The grid topology of the emulated power system is exactly the same than the resistive network B and C.



**Figure 3:** Imaginary current is related to real current in network C



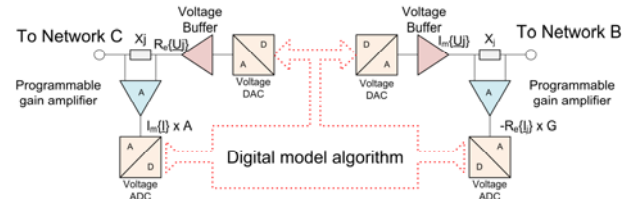
**Figure 4:** Real current is related to imaginary current in network B

#### 4.2 Interfaces connected to a node

Two different interfaces have been developed in order to connect to each node of the emulated grid. Therefore, each node is contained in the network B and network C

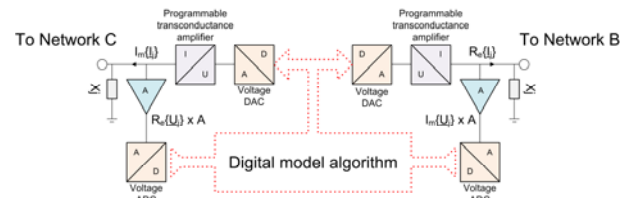
domain at the same time. Both interfaces presented below aims to sense the power injected in the node and are sufficient for emulating all types of generator and load models. Then, both interfaces are connected to a feedback algorithm able to compute the complex currents or voltages from the complex magnitudes sensed on the node. The implemented algorithm models the electro-mechanical equations of generator and load equations by means of a differential algebraic equation (DAE). Different model algorithms that can be implemented with those interfaces are presented in chapter 5.

The first interface (presented in Fig. 5) is dedicated to emulate a slack generator but can also be used for other generator and load models. Feedback is provided on the complex voltage  $\underline{U}_j$  from the sensing of the complex current  $\underline{I}$  injected in the grid. The feedback algorithm depends on the implemented model. The variation of the voltage  $\underline{U}_j$  is sensed by the rest of the grid though the transmission line  $X_j$ . This first described interface is called the voltage model interface.



**Figure 5:** Complex voltage model interface

The second interface (Fig. 6) is based on the same principles and called the current model interface. Feedback is provided on the complex voltage  $\underline{I}$  from the sensing of the complex voltage  $\underline{U}_j$ . This interface is used in all types of load models and can also be used for generator models.



**Figure 6:** Complex current model interface

Now that the theoretical points related to the PE approach have been presented, the next chapter is devoted to listing algorithms that model different components of the power system.

## 5 GENERATOR AND LOAD MODELS

A restricted set of generator and load models has been chosen in order to be implemented on both hardware prototypes. Therefore, three models of load and two models of generators have been selected. We begin by describing the load algorithm models; then the generator models are presented.

### 5.1 Load models

The first load model implemented in [2] was not sufficient to accurately represent a long-term phenomenon of a real power system because the real loads are modeled as a

mix of three different load types: the constant impedance load, the constant power load and the constant current load [7]. Thus two enhanced load models have been included in order to improve the features of the mixed-signal emulator.

The *constant impedance load* is modeled by using the complex current model interface (Fig. 6). Complex currents injected into the node are related to the admittance and the measured complex voltage of the node. The feedback algorithm is presented in (2).

$$\begin{aligned}\Re\{\underline{I}_{li}\} &= \Re\{\underline{Y}_{li}\} \cdot \Re\{\underline{U}_{li}\} - \Im\{\underline{Y}_{li}\} \cdot \Im\{\underline{U}_{li}\} \\ \Im\{\underline{I}_{li}\} &= \Re\{\underline{Y}_{li}\} \cdot \Im\{\underline{U}_{li}\} + \Im\{\underline{Y}_{li}\} \cdot \Re\{\underline{U}_{li}\}\end{aligned}\quad (2)$$

The modeling of the *constant power load* is also realized with the complex current model interface (Fig. 6). The complex currents injected into the node is related to the active and reactive power and the measured complex voltage of the node. The feedback algorithm (3) is as follows:

$$\begin{aligned}\Re\{\underline{I}_{li}\} &= \frac{P_{li} \cdot \Re\{\underline{U}_{li}\} + Q_{li} \cdot \Im\{\underline{U}_{li}\}}{\Re\{\underline{U}_{li}\}^2 + \Im\{\underline{U}_{li}\}^2} \\ \Im\{\underline{I}_{li}\} &= \frac{P_{li} \cdot \Im\{\underline{U}_{li}\} - Q_{li} \cdot \Re\{\underline{U}_{li}\}}{\Re\{\underline{U}_{li}\}^2 + \Im\{\underline{U}_{li}\}^2}\end{aligned}\quad (3)$$

The modeling of the *constant current load* is straightforward and also based on the complex current model interface (real part and imaginary part of the current injected into network B and C). This model doesn't need any feedback related to the complex voltages measured on the node as complex current are constant during the simulation.

## 5.2 Generator models

Both generator models include the computation of the swing equation (6). The *classical model* (model 1.0) of the generator can be implemented using both interfaces presented in section 4.1. Indeed, the classical model of the generator needs to compute the active power injected into the grid (5). The power stems from the magnitude of the complex current injected in the node and also from the magnitude of the complex voltage of the node. The feedback algorithm of the classical model of the generator is as follows [4].

$$P_e = \Re\{\underline{U} \cdot \underline{I}^*\} = \Re\{\underline{U}\} \cdot \Re\{\underline{I}\} + \Im\{\underline{U}\} \cdot \Im\{\underline{I}\} \quad (5)$$

$$\frac{2 \cdot H_i}{\omega_0} \cdot \frac{d^2 \delta_i}{dt^2} = P_m - P_e \quad (6)$$

$$\Re\{\underline{I}_{gi}\} = \cos(\delta_i) \cdot \frac{E'_i}{x'_d} \quad (7)$$

$$\Im\{\underline{I}_{gi}\} = \sin(\delta_i) \cdot \frac{E'_i}{x'_d} \quad (8)$$

$\delta$  = electrical generator angle [rad]

$H_i$  = inertia of the generator [s]

$\omega_0$  = angular frequency of the power system [rad / s]

$P_e$  = active power of the generator provides to the network [pu]

$P_m$  = mechanical power provides to the generator [pu]

The validity of the classical generator results is limited to a short time (~5s) after a sudden topology change because the internal voltage of the generator is maintained constant. This drawback strictly limits the category of scenarios that can be emulated. To emulate long-term scenarios, such as stability analysis of voltage and frequency, more advanced generator models are required. This limitation can be removed by using Parks generator model equations. In this more complete generator model, additional phenomena are modeled. More precisely, the classical swing equation (9) is completed by several additional equations: the excitation winding in the direct axis (12), the damper winding in the quadrature axis (13), the algebraic stator (14) and (15). An implicit damping related to the oscillations of the electrical generator angles (12) and (13) is therefore modeled. Note that a further enhancement of the generator model can be achieved by adding controllers as automatic voltage regulators (AVR) and governors (GOV) [4].

$$\begin{bmatrix} U_q \\ U_d \end{bmatrix} = \begin{bmatrix} \cos \delta & \sin \delta \\ -\sin \delta & \cos \delta \end{bmatrix} \cdot \begin{bmatrix} \Re\{\underline{U}\} \\ \Im\{\underline{U}\} \end{bmatrix} \quad (9)$$

$$P_e = U_q \cdot I_q + U_d \cdot I_d \quad (10)$$

$$\frac{2 \cdot H_i}{\omega_0} \cdot \frac{d^2 \delta}{dt^2} = P_m - P_e \quad (11)$$

$$\frac{dE'_d}{dt} = \frac{1}{T'_{d0}} [-E'_d - (x_q - x'_q) \cdot I_q] \quad (12)$$

$$\frac{dE'_q}{dt} = \frac{1}{T'_{q0}} [E_{fd} - E'_q + (x_d - x'_d) \cdot I_d] \quad (13)$$

$$I_d = -\frac{E'_q - U_q}{x'_d} \quad (14)$$

$$I_q = \frac{E'_d - U_d}{x'_q} \quad (15)$$

$$\begin{bmatrix} \Re\{\underline{I}_{li}\} \\ \Im\{\underline{I}_{li}\} \end{bmatrix} = \begin{bmatrix} \cos \delta & -\sin \delta \\ \sin \delta & \cos \delta \end{bmatrix} \cdot \begin{bmatrix} I_q \\ I_d \end{bmatrix} \quad (16)$$

$\Re\{\underline{U}\}, \Im\{\underline{U}\}$  = generator output voltage in grid reference [pu]

$\Re\{\underline{I}_{li}\}, \Im\{\underline{I}_{li}\}$  = generator output current in grid reference [pu]

$U_d, U_q$  = generator voltage output components in the direct / quadrature axis [pu]

$I_d, I_q$  = generator current output components in the direct / quadrature - axis [pu]

$E'_d, E'_q$  = generator internal voltages components in the direct / quadrature - axis [pu]

$x_d, x_q$  = direct / quadrature - axis synchronous reactances [pu]

$x'_d, x'_q$  = direct / quadrature - axis synchronous transient reactances [pu]

$E_{fd}$  = Exciter voltage referred to stator [pu]

$T'_{d0}, T'_{q0}$  = direct / quadrature - axis transient open circuit time constant [s]

The next chapter is related to the validation of the model presented above through a reference power system topology. Results provided by a dedicated microelectronic behavioral simulator are compared with EUROSTAG [8].

## 6 VALIDATION OF THE IMPLEMENTED MODELS

The simulation of the models described above is necessary for a suitable and accurate validation. Therefore, a reference topology with a given scenario has been chosen. The topology contains three generators and a load. The disturbance initiating the transient event is a three-phase fault occurring in the middle of the line between generator 2 and the load. The fault is cleared after three and a half cycles (70 [ms] at 50Hz). The scenario is simulated through the steps shown in Fig. 7:

- a) Emulation of the steady state conditions using the values computed through load flow
- b) Occurrence of the three phases short-circuit between G2 and L1 in the middle of this transmission line.
- c) Disconnection of the short-circuited transmission line after a predefined time.

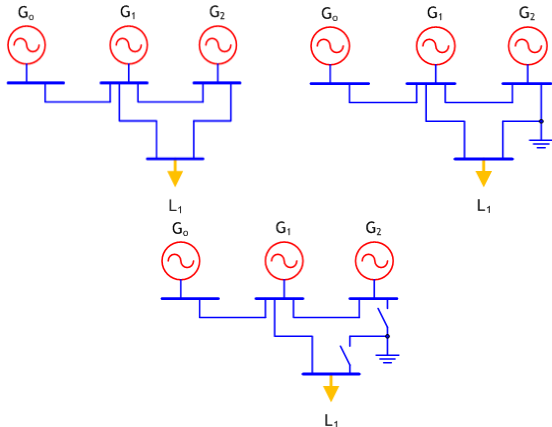


Figure 7: Scenario applied to the reference topology

The topology as well as the scenario have been implemented with Mentor graphics tools. The generator model uses the Park generator equations and the load model is the constant impedance model. Mentor graphic ADVance-MS simulator and VHDL-AMS behavioral language is chosen because this language is the normal flow when starting a mixed-signal front-end design. Indeed, it is much faster to simulate first order effects depicted by an efficient behavioral model in VHDL-AMS than starting with sophisticated models of transistors building the interface blocks (DAC and ADC). Comparison results obtained with ADVance-MS and EUROSTAG are shown in Fig 8. Only the rotor angles of generator 1 and 2 are shown. Indeed, the generator 0 is used as phase reference.

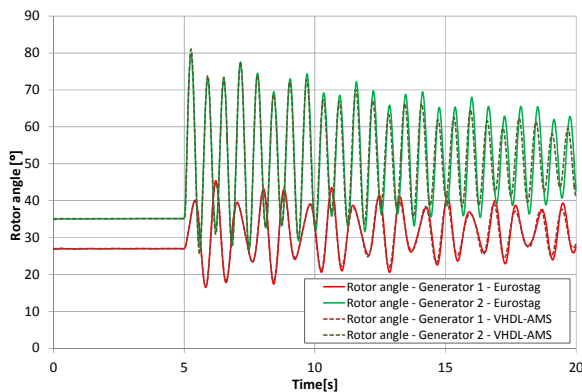


Figure 8: Rotor angles for the generator 1 and 2 computed with EUROSTAG and VHDL-AMS

Fig. 8 shows that the ADVance-MS software containing our implemented models provides very accurate results during the five seconds following the fault. Nevertheless, there is an over-damping in the results provided by the ADVance-MS simulation. This is more clearly seen in Fig. 9 where the differences between the ADVance-MS and EUROSTAG simulation results are plotted. We can see that the differences clearly increase over time. This is

due to EUROTAG using a different numerical solving method from ADVance-MS; furthermore, explicit methods of integration usually over evaluate the generator angle damping [8].

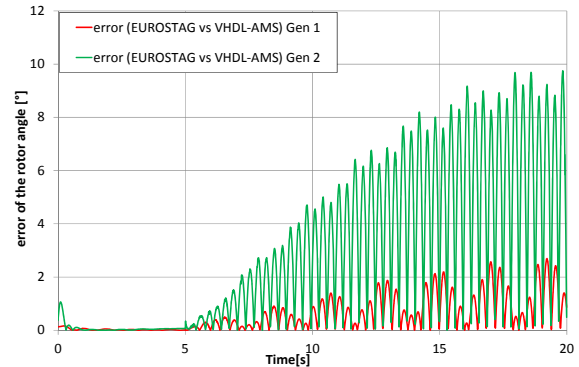


Figure 9: Difference between the rotor angles computed with ADVance-MS and EUROSTAG

Tab.1 shows the differences between both simulators in term of solving and integration method. Nevertheless, results accuracy is sufficient for security assessment which is the role of such a computer at the first attempt.

	ADVance-MS	EUROSTAG
Solving method	Partitioned	Simultaneous
Integration method	explicit	implicit
Variable time step	Yes	Yes

Table 1: Comparison between ADVance-MS and EUROSTAG solving and integration method

## 7 TWO HARDWARE IMPLEMENTATIONS BASED ON THE PHASOR EMULATION (PE) APPROACH

Both hardware realizations are based on plug-and-play PCBs. Both realizations contain the necessary features to provide either a complex voltage or complex current model interface. The digital model algorithms of the aforementioned models are implemented on an embedded 32bit processor. Therefore each board contains three blocks that are connected to the embedded processor: a feedback adjustment, a sensing and a transmission line emulation block.

The main difference between these two realizations is the type of electronic components from which they are built. The first board (Fig. 11) contains an interface build with discrete components. It is the first realization that aims to validate the FPPNS concept on hardware. The second board (Fig.12) contains two dedicated application specific integrated circuits (ASIC). This second realization anticipates a full integrated emulator containing tens of atoms on the same substrate. The goal of the second is obvious: it greatly increases the signal-to-noise ratio and the area reduction of the circuit board by means of a dedicated and integrated solution. A simplified schematic of the features of both circuits is shown in Fig.10 here below.

The design process chosen is AMS 0.35 $\mu$ m technology because it includes a high-poly resistive layer. Such tech-

nology allows the realization of the programmable transmission lines that emulate the grid. All functionalities of a half atom have been designed and are implemented on a single chip. It can be used either as a complex voltage or complex current model interface. The feedback adjustment, sensing and transmission line emulation blocks have been designed and connected together in the ASIC version. The layout of the realized circuit is shown in Fig.10.

The ASIC uses 128 analog switches used amongst others in order to configure the atom (amplifiers gain, type of interface and impedance of the transmission lines). A high-speed serial-to-parallel interface (SPI) has been designed for this purpose aiming to reduce the number of pads of the circuit. The specifications of both PCBs are presented in Tab 2.

Parameter	Discrete component PCB	Integrated component PCB
Voltage scale	1 V/pu	1 V/pu
Current scale	4uA/pu	1uA/pu
Impedance scale	250kΩ/pu	1MΩ/pu
ADCs specs	10-12 bit@100–500kS/s	10 bit@ 100kS/s
DACs specs	12 bit@100kS/s	10bit@1MS/s
MAX speed	100x faster than real-time	100x faster than real-time

Table 2: Main specifications of the two presented PCB hardware

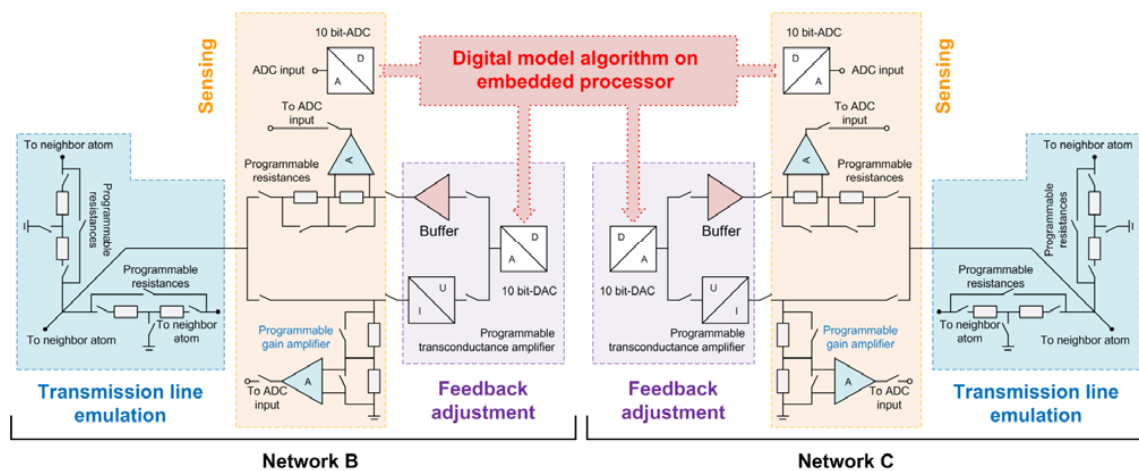


Figure 10: Simplified schematic of both PCB features

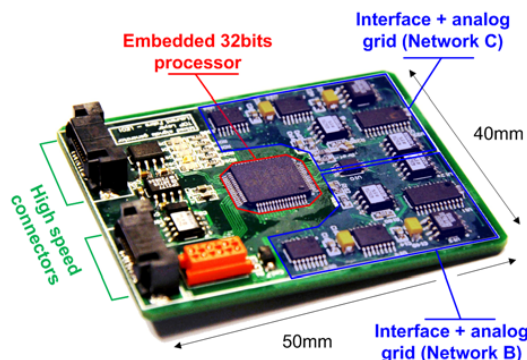


Figure 11: PCB atom realization containing discrete components

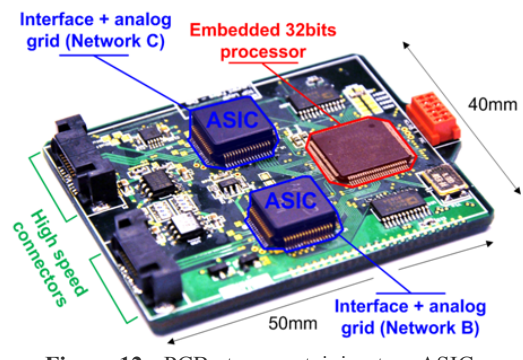
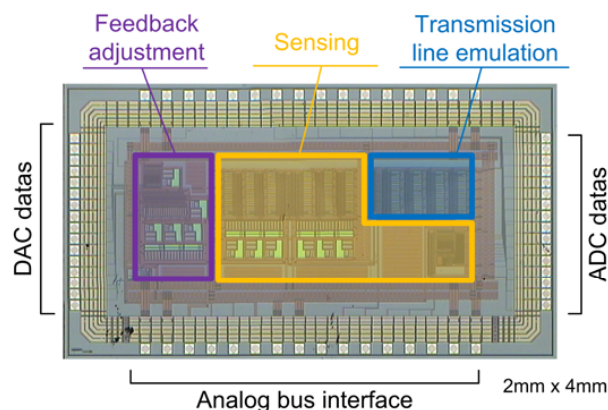


Figure 12: PCB atom containing two ASICs



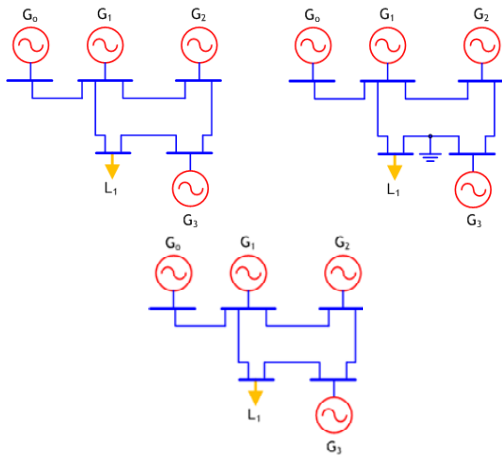
**Figure 13:** Floorplan of the first dedicated ASIC for power system emulation

## 8 COMPARISON: DIGITAL SIMULATION VS MIXED-SIGNAL EMULATION

Two different scenarios have been simulated and emulated taking a five-node reference topology. The implemented models are the generator model 1.0 and the constant impedance load model.

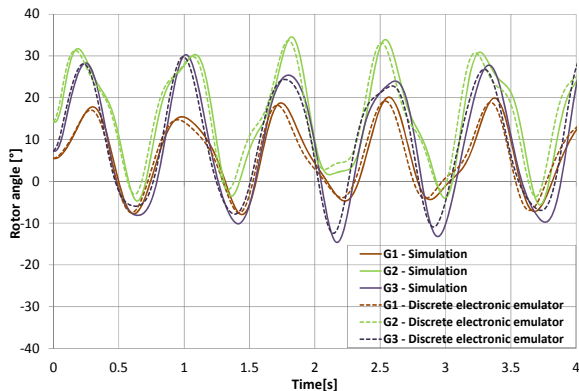
### 8.1 First scenario comparison

The first comparison scenario executed is depicted in Fig. 14:

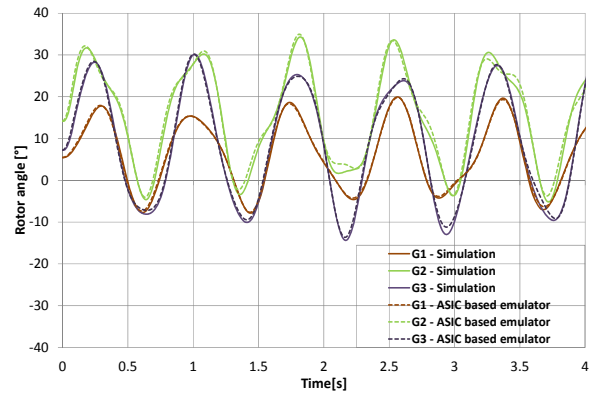


**Figure 14:** First applied scenario (a) Steady state emulation (b) Three phase fault (c) Restoring connection after 70ms

Fig. 15 and Fig. 16 compare the results of both hardware circuits with the results of a reference digital simulator for the first scenario. The rotor angle oscillations of generators  $G_1$ ,  $G_2$  and  $G_3$  are shown using  $G_0$  as an angular reference.



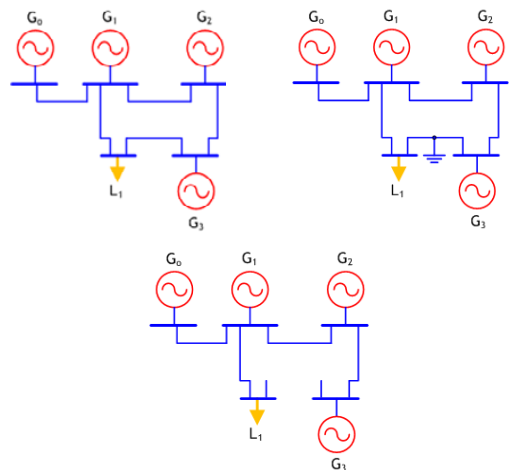
**Figure 15:** Rotor angles oscillations for the first scenario. Comparison between simulation and discrete electronics emulation



**Figure 16:** Rotor angles oscillations for the first scenario. Comparison between simulation and ASIC build emulation

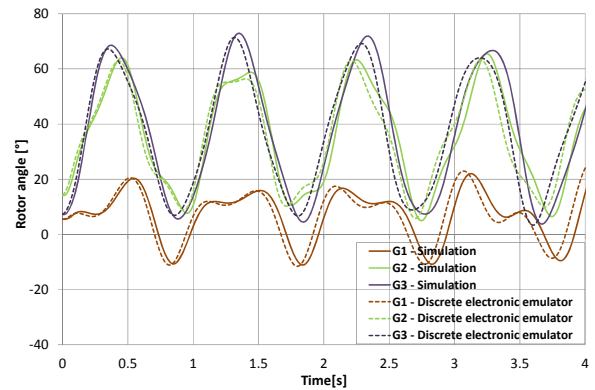
### 8.2 Second scenario comparison

The second comparison scenario executed is shown in Fig. 17:

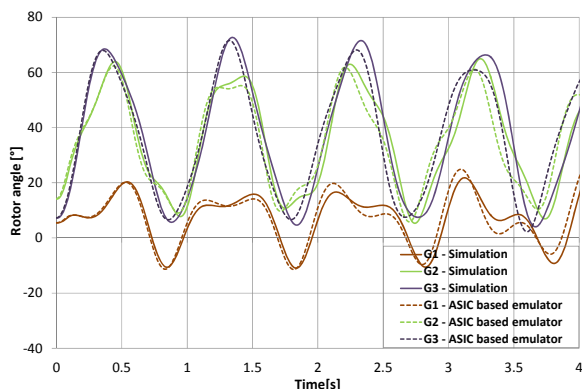


**Figure 17:** Second applied scenario (a) Steady state emulation (b) Three phase fault (c) Disconnection after 70ms

As previously, both hardware results are presented and compared with a reference digital simulator (Fig. 18 and Fig. 19). The rotor angle oscillations of generators  $G_1$ ,  $G_2$  and  $G_3$  are shown using  $G_0$  as an angular reference.



**Figure 18:** Rotor angles oscillations for the second scenario. Comparison between simulation and discrete electronics emulation



**Figure 19:** Rotor angles oscillations for the second scenario. Comparison between simulation and ASIC build emulation

### 8.3 Discussion

The comparison between the digital simulation and both mixed-signal hardware emulation prove that the hardware circuits are precise and accurate. Moreover, the emulation speed used for the mixed signal emulation results was 100x faster than real time for the four comparison schemes. Therefore, an emulation time of 4 seconds in real power world represent an emulated time of 40ms. The PCB area of both reconfigurable atoms is the same for the discrete and integrated realization. Nevertheless, the active element representing an integrated atom is contained in 2mm<sup>2</sup>. The integrated solution is consequently well dedicated for a system-on-chip integration.

## 9 CONCLUSION

This paper presents two circuits based on the described FPPNS concept and is based on a mixed-signal implementation. They can emulate any power system topology. Both circuits are using the Phasor Emulation (PE) approach. The first PCB uses purely discrete electronics and the second realization is based on our first designed ASIC. Both circuits can be plugged directly on a development platform allowing the emulation of a topology that contains up to 16 nodes and up to 32 branches. The comparison between digital simulation results and both mixed-signal emulation results have been provided. The ASIC version of the atom prove that a multiple integrated node system is possible. Furthermore, the precision and accuracy of such a system is sufficient for the computation of dynamic security assessment. Speed is currently limited by the ADCs and DACs conversion time and thus the speed is restricted to under 100 times faster than real time without accuracy reduction.

The authors started the achievement of a new mixed signal hardware platform able to emulate up to 5'000 times faster than real-time with the same concept. High speed ADCs and DACs will be specially designed and used for this purpose. In the same time they will increase the number of nodes able to be emulated on the same platform. A fully integrated version will soon be available

applying FPPNS principle with more than 100 atoms. The author targets an active area of 1mm<sup>2</sup>/atom.

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