A Resynchronization Algorithm for Topological Changes in Real Time Fast Transients Simulation

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Abstract - To guarantee the synchronization between the digital simulation and the associated equipment that interfaces it with the real world, as well as to reduce the computational burden necessary during every integration step, real time digital simulation of electric power networks rely on the use of constant-size integration steps. The network state is determined only at certain equidistant points along the time axis, the deadline-rendezvous points. These series of rendezvous points mark the synchronism between the simulator and the real world. Changes of the network topology occur, however, asynchronously with respect to that stream of samples. In simulators of the EMTP type, accounting for those topological changes is currently postponed until two deadline-rendezvous points later. This delay introduces unacceptable errors in the simulation, particularly in cases with an intense switching as in the case of simulation of power electronics devices. In this paper, a new method with reduced computational overhead and no prediction, for the inclusion of those topological changes as soon as possible, is introduced.

Keywords - EMTP simulation of power electronic devices, switching asynchronous events in fixed time steps simulators, numerical oscillations in circuit solutions, real time simulations, the OVNI simulator.

1 Introduction

THE search for a digital solution to real time simulation of power networks has naturally orbited around the ubiquitous Electromagnetic Transients Program, the EMTP [4], as is evident from the simulators described in [13], [10], [3], [7].

To guarantee the synchronization between the digital simulation and the associated equipment that interfaces it with the real world, as well as to reduce the computational burden necessary during every integration step, real time digital simulation of electric power networks rely on the use of constant-size integration steps.

To simulate a power network in real-time, the engine computes and issues the status of the system at evenly spaced intervals of time, i.e., it issues the output data at a constant sampling rate. How the actual computation proceeds is transparent to the external real world, as long as the right data comes out of the simulator at each of those evenly spaced deadline-rendezvous points, DRP.

However, a constant integration step simulation (CISS) takes snapshots of the system only at the deadline-rendezvous points. Topological changes, introduced by switching devices or by piecewise representations of nonlinear elements, that occur between any two DRPs are not accurately represented. Switching operations are essentially asynchronous with respect to the simulation data stream. CISS delivers results whose acceptability depends on the case simulated, as detailed in what follows.

1.1 *Defects introduced by Asynchronous Switching Operations.*

In EMTP simulations, the detection of the conditions for a switch to operate is made at the first integer simulation step after the actual switch operation . As an example, when an AC-switch is signaled to open, the switch will open only when its current becomes zero in the natural process of the circuit solution, Fig. 1.

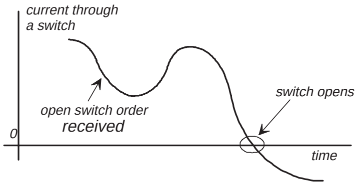

Figure 1: Switch opening event: signal, and actual opening.

In EMTP-type simulations the detection of the *zero crossing* occurs when the current through the switch waiting for opening changes sign, at t_b in Fig. 2, [5]. To avoid the additional computational overhead associated with going back to t_a and advancing with a appropriately reduced integration step to the exact point where the zero crossing occurs, the actual zeroing of the current through the switch is not made until the next integration step after the *zero crossing* is detected, at t_c in Fig. 2.

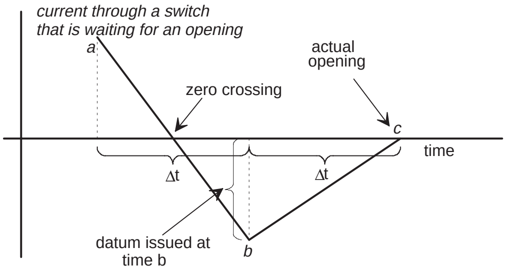

Figure 2: Zero crossing and actual opening of a switch.

There is an interval of time during which the network topology is not mirrored by the simulation. In most cases, this is an acceptable and efficient solution, given small enough integration steps.

However, in situations where the accurate representation of the network topological structure is essential to the correctness of the simulation, as in power electronics simulations where a topological change may trigger a very close subsequent topological change, such delay cannot be tolerated anymore. Two examples of the problems incurred by this method are included in section 5.

2 Resynchronization of Switching Operations

In non-real-time simulations, a possible solution is to *backtrack* to the actual moment when the zero crossing occurred, and issue the data at that particular moment in time, with the time stamp of the actual zero crossing itself. The result is a shortened integration step right before the opening of the switch. After that, the simulation can proceed at the regular integration step. The result would be that all future samples get slightly *shifted* to the left, Fig. 3. This is unacceptable in real-time simulation, since the process would lose synchronism with the external real-time clock.

This is also an expensive proposition. The simulation assumes that the monitored current in the switch varies linearly between points a and b' in Fig. 4, to find the *crossing time* b. Then it goes back to a and advances again, this time with the shortened integration step $\Delta t_{short} = b - a$. This shortened integration step implies recalculation and retriangularization (or inversion) of the network matrix. All this almost doubles the computational effort of this solution step.

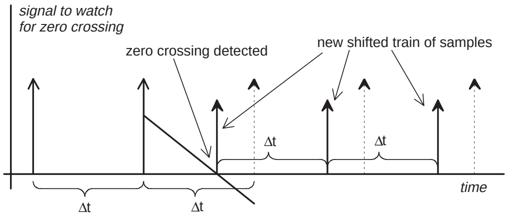

Figure 3: Non real time backtracking.

2.1 *Real-Time Resynchronization*

In real-time simulations, instead, the OVNI [12] [14] simulator[1] uses the already known data at a and b', and interpolates linearly to obtain not only $t = b$ (the time stamp of the zero crossing), Fig. 4, but also the value of every node voltage and every history source at the zero crossing point, b. This produces the complete status of the system at the crossing point. But the crossing point is not among the prescheduled solution points[2] of the interface between the simulator and the external equipment. In OVNI, a compromise is made, Fig. 4. Instead of releasing the completely wrong value at b' of each variable $x(t)$[3], $x(b')$, a lesser evil approach is taken, the correct value[4] at the zero crossing, $x(b)$, is issued slightly later, on the next rendezvous point, at b'.

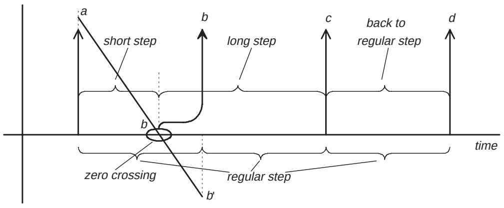

Figure 4: Simple non regressive backtracking.

The problem is now how to advance from b up to c in Fig. 4. One possibility, see Fig. 5, is to use the available matrices for Δt and advance computationally from b to c', and then use linear extrapolation to reach the values needed at c, where they are issued. Then the simulation resumes. This is the solution reported in [1]. A source of concern with this technique, however, is the prediction involved in the procedure (even though small).

A method with no prediction, the subject of this paper, is presented next.

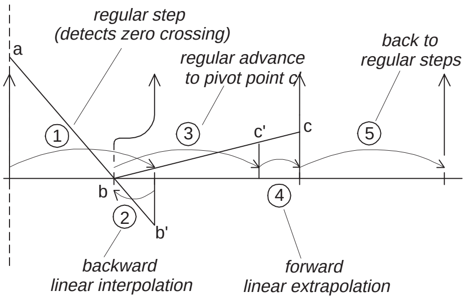

Figure 5: BIFE: Backward interpolation, forward extrapolation.

3 Integration Rules and DSDI

Central to the method to be introduced here are the characteristics of the two integration rules utilized: Backward Euler and Trapezoidal; they are called BE and TR in what follows.

BE is the backbone of DSDI (also dubbed CDA-inverse because of the reversed order of roles played by BE and TR), the double-step double-interpolation method presented in this paper. At topology change points, DSDI switches momentarily to TR and then back to BE, as will be detailed in section 4. With BE, only state variables[5] appear in the initial conditions of the integration process. This is important since only state variables can be predicted accurately for resynchronization of the simulation with the real-time stream [1]. If TR were to be chosen,

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[1] OVNI = Object Virtual Network Integrator, the real-time simulator which is the flagship of the research at the Real-Time Simulation Laboratory at U.B.C.

[2] i.e., the “rendezvous” points.

[3] Where $x(t)$ represents here any node voltage, or history source value.

[4] “Correct value” obtained by linear interpolation of the network state between the last two solution points.

[5] Voltage in capacitors and current in inductors

variables which are not state variables would need to be included among the initial conditions.

BE can simulate the behaviour of the system across discontinuities more correctly than TR [9]. A simulation of a switching power electronics circuit presents the algorithm with a continuous sequence of discontinuities, so a sustained use of BE gives better results for this type of simulation.

BE was also the choice in the HVDC model of [2] because of its critical damping properties, which are essential to suppress numerical oscillations during switching operations (CDA technique, [9]).

As shown in [9], for the same integration step Δt, the elements of the equivalent discretized network matrix produced by BE, $[G_{BE}]$, have a value of two times the corresponding element produced by TR, $[G_{TR}]$. An alternative way of looking at that is *"the conductance matrix produced by BE with an integration step Δt is identical to the conductance matrix produced by TR with an integration step twice as big $2\Delta t$".*

4 Double Step Double Interpolation Concept, DSDI

For the reasons explained, OVNI uses the backward Euler rule for the normal solution steps of the switched power electronic devices. When a zero crossing, or a topology change, is detected at the end of an integration interval, b' in Fig. 6, the DSDI technique uses backward linear interpolation between the last two sets of values (at a and b') to establish the state of the network at the point of topology change, b. The status of the network is output on the rendezvous point at b'.

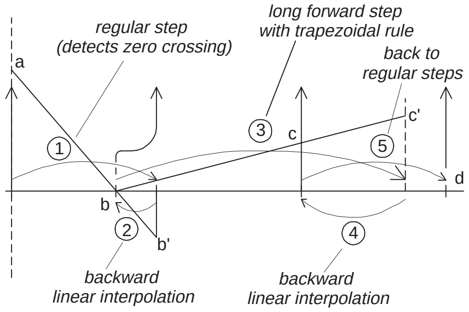

Figure 6: DSDI used in OVNI. The most expensive step takes one regular integration step with precalculated matrices, plus one inexpensive linear interpolation.

At this point, DSDI switches to TR to evaluate the elements history sources while still using the same network matrix as with BE. The effect of this, as seen in the previous section' is to advance the simulation by a double-size integration step, up to c' in Fig. 6. DSDI then interpolates linearly between the status of the network at b and c' to establish the actual status at the next DRP in the stream, the one at c.

As is evident from the figure, there is no need for double recalculation of the $[G]$ matrix per integration step, and also the second rendezvous point data is obtained by interpolation. In short, the overhead per integration step is only that of the linear interpolation.

4.1 Efficiency issues

In real-time simulations the efficiency of the method is as important as its accuracy. The real-time deadline imposes a rigid border on the computational meanders of the algorithm. The DSDI algorithm was conceived with that deadline as a goal.

The computational efficiency of the algorithm can be assessed as follows. For a network with n nodes and h history sources (once it has been discretized), evaluating the system status by integration of the equations requires a number of floating point operations (flops) given by

$$k_h > 3h \tag{1}$$

flops, to update the history sources[6]. And, to solve the node voltages, it is necessary an additional

$$k_{full} \approx 3h + n^2 \tag{2}$$

flops. On the other hand, to obtain the status of the same network by linear interpolation, the requirement lowers to

$$k_{inter} = 3(n + h) \tag{3}$$

flops. Each of the steps where DSDI is necessary requires a total number of flops

$$k_{DSDI} = k_{full} + k_{inter} \tag{4}$$

The percentage increase of time per step introduced by DSDI is

$$penalty = \frac{k_{DSDI} - k_{full}}{k_{full}} 100\% \tag{5}$$

$$k_{inter} = 3(n + h) \;\; flops. \tag{6}$$

Figure 7 shows the penalty incurred by DSDI, computed as in (5), for a number of nodes ranging from 20 up to 200. The lowest curve corresponds to a purely resistive network (no history sources).

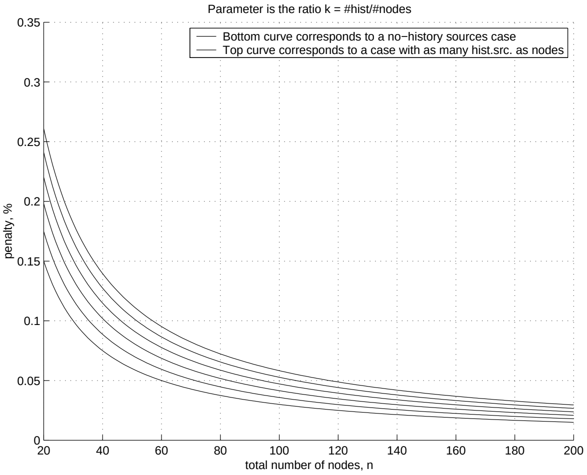

Figure 7: Penalty in percentage incurred by DSDI for network with different number of nodes and history sources.

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[6] Under the assumption of minimum complexity in this process, as in an inductor.

Each of the other curves correspond to networks with an increasing number of history sources, up to the top one which has as many history sources as nodes.

These approximated curves suggest that the penalty introduced by DSDI for networks with more than 40 nodes is less than 15%, and that for networks with more than 60 nodes the penalty is less than 10%.

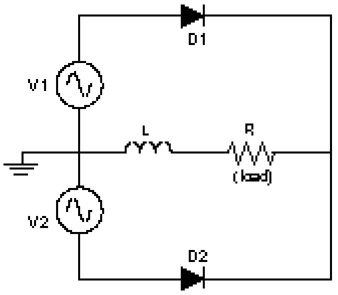

Figure 8: A two-diode full wave rectifier case.

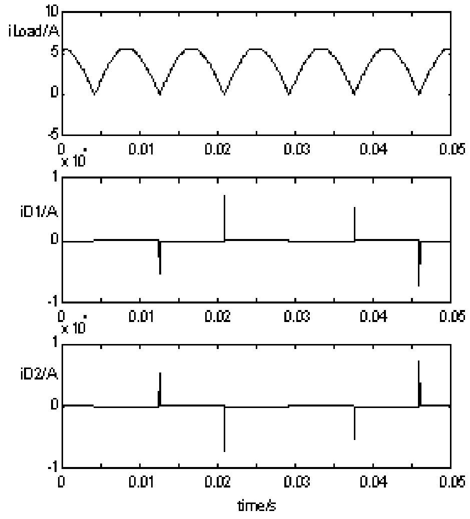

Figure 9: Results of the EMTP for the two-diode rectifier, currents (a) in the load, (b) in diode one, (c) in diode two. Observe the current spikes of several thousand amperes, while the load current peaks at about five amperes.

5 Validation of DSDI

The DSDI algorithm was validated using several different test simulations. Among those tests, two cases were chosen to be included in this paper:

- full-wave two-diode rectifier circuit.
- HVDC substation circuit.

Both cases were run both on the Microtran [11] version of the EMTP as well as on a subset of OVNI [12][14] implementing a prototype of DSDI. All tests correspond to an integration step of $\Delta t = 50\mu s$.

5.1 Full wave two-diode rectifier circuit case

The circuit simulated can be seen in Fig. 8. It includes two sinusoidal voltage sources 180^o out of phase with respect to each other, two diodes $D1$ and $D2$, a smoothing reactor, and the resistive load, with the following values:

$$\begin{array}{lll} V_{ac1} = 200V, & phase(V_{ac1}) = 0^o, & f_{ac1} = 60Hz, \\ V_{ac2} = 200V, & phase(V_{ac2}) = 180^o, & f_{ac2} = 60Hz, \\ R = 50\Omega, & L = 1mH, & x_{33} \end{array}$$

where

V_{ac} : r.m.s. voltage of the a.c. source, volts,
$angle(V_{ac})$: phase of the a.c. source, degrees,
f_{ac} : frequency of a.c. source, hertz.

5.1.1 EMTP simulation

In this circuit, only one diode will be conducting at any one time (ON state), while the other is in its OFF state. Due to the delay in opening a diode when its current crosses zero,

the EMTP solution encounters a pathological topology that does not occur in the actual circuit, namely, that one diode starts to conduct (turns ON), when the other diode has not been put OFF yet. Albeit for one integration step, the EMTP presents a current path of extremely small impedance during that step: large currents in the diodes appear in this simulation, as shown in Fig. 9. The delay in opening the diode produces *current spikes* that are not there in the actual circuit. As can be seen in the graphics for valve currents, the spikes are so large that they obscure completely the shape of the current.

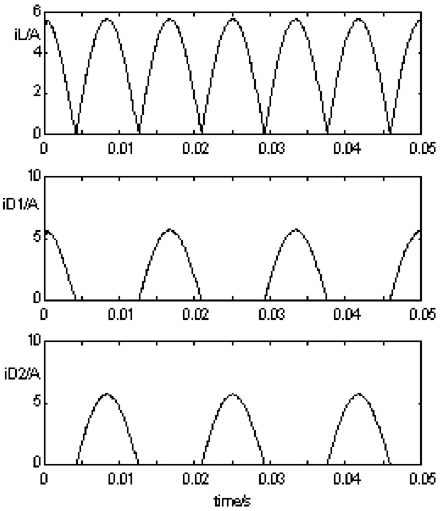

Figure 10: Results of DSDI for the two-diode rectifier, currents (a) in the load, (b) in diode one, (c) in diode two.

5.1.2 DSDI Simulation

The DSDI algorithm produced the results shown in Fig. 10. In this case, no current spikes appear. All currents, both in the load and in the diodes are simulated correctly in this case. At the same time, the real-time clock synchronization has been preserved. The current in the valves, once the spikes have been removed by the DSDI technique, can be perceived as shows in the figure.

5.2 *A six-valve three phase HVDC rectifier*

A case energized by a three phase system of voltages, Fig. 11, feeding a resistive load through a full wave six-valve rectifier bridge and a smoothing reactor was prepared and put to both the EMTP and DSDI.

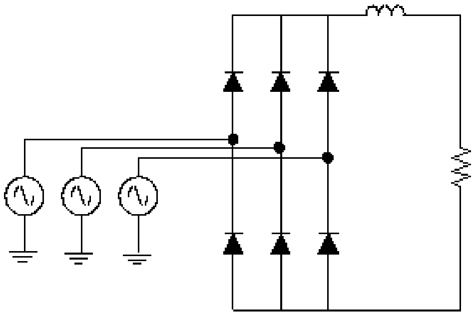

Figure 11: A six-valve HVDC rectifier.

5.2.1 *EMTP Simulation*

Same as in the case of the two-diode full wave rectifier, the EMTP allows valve two go to the ON state, while valve one has not been put OFF yet. Again, current-spikes flow in the simulation that have no counterpart in the actual circuit, Fig. 12.

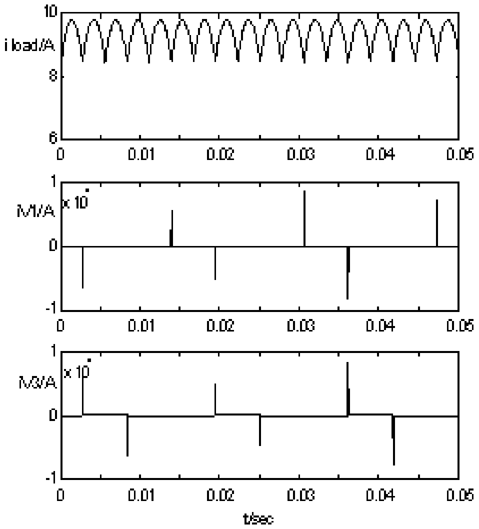

Figure 12: EMTP results of six-valve HVDC rectifier, currents (a) in the load, (b) in valve one, (c) in valve two.

5.2.2 *DSDI Simulation*

The DSDI algorithm opens valve one right on time to prevent the occurrence of the low impedance path found in the previous section. In this case, DSDI produces the correct values for the currents in the valves. Valve currents are free of current spikes, Fig. 13.

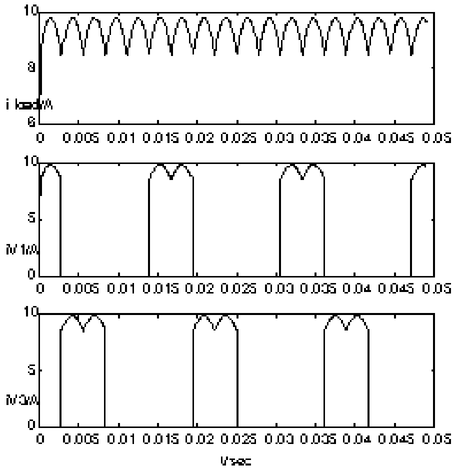

Figure 13: Results of DSDI for the six-valve HVDC rectifier, currents (a) in the load, (b) in diode one, (c) in diode two.

6 Conclusions

A new algorithm, the Double-Step Double Interpolation concept, DSDI, has been implemented into a real-time solution that models accurately and efficiently the changes of topology in the network in a real-time fast electromagnetic transients simulation.

The algorithm accounts for structural changes in the network right at the instant at which the monitored signals meet the conditions for the changes to occur. DSDI does so through the linear interpolation of nodal voltages and history sources (state variables) back to the instant of topology change.

DSDI achieves resynchronization with the real-time clock at the next integration step at which no change in topology is detected. Resynchronization is obtained by a switch of integration rules, from the Backward Euler being used throughout the simulation down to the Trapezoidal rule for one integration step, to advance a double-size integration step with the same set of matrices, plus another interpolation of nodal voltages and history sources. This process is exactly the “dual” of the simulation process in the EMTP with the CDA technique, where trapezoidal rule is normally used and the simulation is switched to backward Euler for two half-size integration steps at switching operations to eliminate numerical oscillations.

The penalty introduced by the additional interpolation at the steps where DSDI becomes active is small enough as to preserve the real-time bandwidth of the simulation. Validation tests focused on a couple of cases simple enough to admit discrete identification of the mechanisms producing false-spikes in the EMTP algorithm and showed the accuracy of the DSDI solution.

DSDI, given its accuracy and efficiency, is suited for inclusion in the solution algorithm of real time simulators for power system electromagnetics transients.

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